REMARKS/ARGUMENTS

Applicants have studied the Office Action dated July 01, 2005. No new matter has been added. It is submitted that the application is in condition for allowance. Applicants have amended claims 1 and 9-11. By virtue of this amendment, claims 1-14 are pending. Reconsideration and further examination of the pending claims in view of the above amendments and the following remarks is respectfully requested. In this Office Action, the Examiner:

(2-3) Rejected claims 1-14 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; and

(4-5) Rejected claims 1-14 under 35 U.S.C. §103(a) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798) in view of Shimotsusa et al. (U.S. Publication No. 2004/0046211) and in further view of Harrington, III (U.S. Patent No. 4,943,537).

Overview of the Present Invention

The present invention provides a delay element for use in integrated circuits that increases parametric tracking of device characteristics, increases chip yield, and provides for enhanced modeling of circuit designs. Electronic circuit designs typically include arrangements for synchronizing operations of digital circuits. It is common to provide one or more clocks for control of the timing operation of most digital circuits. However, a complicating factor in the design of digital circuits is that clock signals are subject to propagation delays and other forms of distortion as they are distributed to various elements of a digital circuit. Typically, electronic delay elements are used on integrated circuits to adjust path timing or to generate extended pulses used for clocking imbedded arrays.

Elements that can generate extended delays are difficult to design and fabricate.

One traditional delay element comprises a series of inverter gates. These inverter delay line configurations used significantly more space (approximately four times) and more power than the conventional type of delay element.

Also, prior art delay elements use various channel length devices which create problems in the modeling and processing of integrated circuits. Typically in production, the process is "tuned" to be optimal for a given channel length. Consequently, this results in variations of channels that are outside the "tuned range." The process in the prior art cannot be tuned to accommodate these high degrees of variation.

Across chip length variation (ACLV) typically is a fixed number in a production process. For example, an 80-nanometer channel length with a tolerance of 10-nanometer yields a 10/80 (12.5%) variation across chips. Compare this to an extended channel length of 280 nanometers, which provides a tolerance of 10/280 or 3.6%. This mixture of channel lengths results in non-uniform tolerance variations across the circuit. Accordingly, the tolerances across the delay stages will not properly track the tolerances of other circuits on the chips. This is especially a problem with timing elements, since delays through delay circuits with extended channel lengths will vary across the chip by a different amount than other circuits with all minimum length elements.

The present invention overcomes the problems discussed above with the prior art by providing a delay element for use in integrated circuits. The delay element includes uniform channel length transistors, thereby increasing parametric tracking of device characteristics, increasing chip yield, and providing for enhanced modeling of circuit designs. To more clearly point out the advantages of the present invention. The Applicants have amended independent claims 1 and 9-11 to recite "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;

wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip".

No new matter has been added. Support for this amended language is found in the application as originally filed and particularly as outlined in the table below.

CLAIM ELEMENT	SUPPORT
without using extended channel length transistors in the delay stages	Page 3, line 27-29 Page 5, line 9
so that tolerances across the delay stages track tolerance of other circuits on a chip;	Page 3, line 16-18.
increases parametric tracking of device characteristics	Page 3, lines 24-26. Page 5, lines 6-8 Page 6, lines 4-7 Abstract
including delays in timing circuits across the other circuits in the chip	Page 3, lines 9-21 Page 5, lines 6-8 Abstract

(2-3) Rejection under 35 U.S.C. §112, second paragraph

As noted above, the Examiner rejected claims 1-14 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Although the Applicants disagree with the Examiner because support is found at page 6, lines 4-7, the Applicants have amended independent claims 1 and 9-11 to now recite "uniform channel length transistors" instead of "uniform minimum

channel length transistors" to further expedite prosecution of the present invention and not to narrow the scope of the present invention. No new matter was added. The Applicants submit that claims 1 and 9-11 recite in allowable form and the rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claims 2-8 and 12-14 depend from claims 1 and 11 respectively. Since dependent claims recite all of the limitations of the independent claim, the Applicants submit that claims 2-8 and 12-14 are also allowable, and the Examiner's rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

(4-5) Rejection under 35 U.S.C. §102(b) as being anticipated by Sato et al

As noted above, the Examiner rejected claims 1-14 under 35 U.S.C. §103(a) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798) in view of Shimotsusa et al. (U.S. Publication No. 2004/0046211) and in further view of Harrington, III (U.S. Patent No. 4,943,537). Independent claim 1 has been amended to now recite "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip" . Independent claims 9-11 have also been similarly amended. No new matter was added. Support for the amendments is found in the Specification as originally filed. See for example page 3, lines 24-26; page 5, lines 6-8; page 6, lines 4-7; and the Abstract.

The Examiner correctly states on page 4 of the office action that "Sato fails to explicitly disclose the use of uniform minimum channel length transistors

provides uniform tolerance variations across a circuit". However, the Examiner goes on to combine Sato with Shimotsusa stating that:

> *Shimotsusa et al. discloses, In page 16, paragraph [0239], an array of transistors with uniform channel lengths which high reliability can be obtained".*[1] *The Examiner further states "to configure the circuit of Sato et al. with uniform channel length transistors as taught by Shimotsusa et al. so that the transistors can be manufactured without any diffusion in their threshold values thus provides high reliability across the circuit would have been obvious to one of ordinary skill in the art at the time of the invention since Shimotsusa et al. teaches that such configuration would facilitate high yield and high reliability (see Shimotsusa et al. page 16, paragraph [0239]*

The Applicants have amended independent claims 1 and 9-11 to more clearly recite the advantages of the present invention, in particular the advantages obtained by using uniform channel length transistors. Independent claim 1 now recites "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Independent claims 9-11 similarly recite the same.

Shimotsusa specifically discloses at paragraph [0239] that "as a result, the channel lengths of transistors arranged in an array become evenly uniform. Consequently, no size difference owing to alignment is caused, and the MIS type field effect transistors can be manufactured without any diffusion in their threshold values. Moreover a high yield can be realized, and high reliability can be obtained."

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[1] Applicants make no statement whether such combination is even proper.

The present invention on the other hand increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip by using uniform channel length transistors. The Applicants agree with the Examiner that Shimotsusa teaches using uniform channel length transistors for manufacturing/yield purposes. However, manufacturing/yield is not the same as parametric tracking. Yield is one measurement among several of the efficiency in a chip manufacturing process. Manufacturing yield is a reflection of the quality of the manufacturing process and drives cost. The present invention, on the other hand, is concerned with parametric tracking. For example, the manufacturing process naturally varies from wafer to wafer. Designs that use a mixture of channel lengths result in non-uniform tolerance variations across the chip. In contrast the present invention eliminates this problem without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip.\.

Nowhere does Shimotsusa teach, anticipate, or suggest "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip" Accordingly, the present invention distinguishes over Shimotsusa for at least this reason.

The Examiner recites 35 U.S.C. §103. The Statute expressly requires that obviousness or non-obviousness be determined for the claimed subject matter "as a whole," and the key to proper determination of the differences between the prior art and the present invention is giving full recognition to the invention "as a

whole." The Sato reference taken alone or in view of Shimotsusa simply does not suggest, teach, or disclose the patentably distinct limitation of:

> "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip"

The limitations taken "as a whole" in independent claims 1 and 9-11 are not present in Sato taken alone or in view of Shimotsusa. Accordingly, the present invention distinguishes over Sato taken alone or in view of Shimotsusa.

The Examiner goes on to combine to combine Sato with Harrington III stating that Harrington III discloses in column 4, lines 4-9, that:

> *the use of minimum channel length confers several advantages regarding drive capability, on-state series resistance and switching speed. It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the combined circuit of Sato et al. and Shimotsusa et al. with minimum channel length transistor as taught by Harrington, III, for increasing drive capability of the device, decreasing the on-state series resistance and also increasing the switching speed of logic circuits since such circuit arrangement for the stated purpose has been a well known practice as evidences by the teaching of Harrington, III (see Harrington., col. 4, lines 4-9)"*

As stated above, the Applicants have amended independent claims 1 and 9-11 to recite "uniform channel length transistors" instead of "uniform minimum channel length transistors". Therefore, the Applicants believe that Harrington III no longer

is applicable and accordingly, the rejection based on Harrington III is now rendered moot.

Further, when there is no suggestion or teaching in the prior art "...without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip" the suggestion cannot come from the Applicants' own specification. The Federal Circuit has repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings of the prior art. See MPEP §2143 and Grain Processing Corp. v. American Maize-Products, 840 F.2d 902, 907, 5 USPQ2d 1788 1792 (Fed. Cir. 1988) and In re Fitch, 972 F.2d 160, 12 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

Moreover, the Federal Circuit has consistently held that when a §103 rejection is based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in the reference, such a proposed modification is not proper and the *prima facie* case of obviousness can not be properly made. See In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Here the intent, purpose and function of Sato taken alone or in view of Shimotsusa and/or in further view of Harrington is a synchronous memory device. CMOS inverters are included and are formed of at least one p-channel MOS transistor and one n-channel MOS transistor. See Sato at col. 13, lines 48-56 and FIGs. 14A-14B. Shimotsusa, on the other hand, only includes one type of field effect transistor in a "stack", for examine, either an n-channel or a p-channel. See, for example, Shimotsusa at FIGs. 2-3, 12, 14, 16-17, 19, 26, and 29B. Also, Harrington III teaches buried channel regions and does not teach stacks of transistors. Because Sato requires an n-channel and p-channel transistor in a

"stacked" configuration, this combination as suggested by the Examiner destroys the intent and purpose of Sato. In contrast, the intent and purpose of the present invention is to use uniform channel length so that tolerances across the delay stages track tolerance of other circuits on a chip thereby providing uniform tolerance variations and increasing parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip. Accordingly, the combination of Sato and Shimotsusa in further view of Harrington III results in an inoperable system, and the Examiner's case of *"Prima Facie Obviousness"* should be withdrawn.

Furthermore, the Federal Circuit stated in McGinley v. Franklin Sports, Inc., (Fed Cir 2001) that if references taken in combination would produce a "seemingly inoperative device," such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness. In re Sponnoble, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969) (references teach away from combination if combination produces seemingly inoperative device); see also In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (inoperable modification teaches away). Here, Sato teaches a synchronous memory device including CMOS inverters comprised of at least one p-channel MOS transistor and one n-channel transistor. Therefore, the combination of Sato with Shimotsusa and/or in further view of Harrington III to produce the presently claimed invention where uniform channel length transistors are used so that tolerances across the delay stages track tolerance of other circuits on a chip thereby providing uniform tolerance variations and increasing parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip would produce an inoperative device. Accordingly, the combination of Sato and Shimotsusa in further view of Harrington III is improper.

For the foregoing reasons, independent claims 1 and 9-11 as amended distinguish over Sato alone and/or in combination with Shimotsusa and/or in

combination with Harrington III. Claims 2-8, and 12-14 depend from independent Claims 1 and 11 respectively. Since dependent claims contain all the limitations of the independent claims, claims 2-8, and 12-14 distinguish over Sato alone and/or in combination with Shimotsusa and/or in combination with Harrington III, as well, and the Examiner's rejection should be withdrawn.

CONCLUSION

The foregoing is submitted as full and complete response to the Official Action mailed July 1, 2005, and it is submitted that claims 1-14 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of claims 1-14 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants acknowledge the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR §§ 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

The present application, after entry of this amendment, comprises fourteen (14) claims, including four (4) independent claims. Applicants have previously paid for fourteen (14) claims including four (4) independent claims. Applicants, therefore, believe that a fee for claims amendment is currently not due.

Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome, and that all claims in the application are allowable. No new matter has been added. It is believed that the application is now in condition for allowance, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

Respectfully Submitted,

Date: September 8, 2005

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